# Defect Modeling of CNT Interconnects for System-in-Package Application

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# Outline

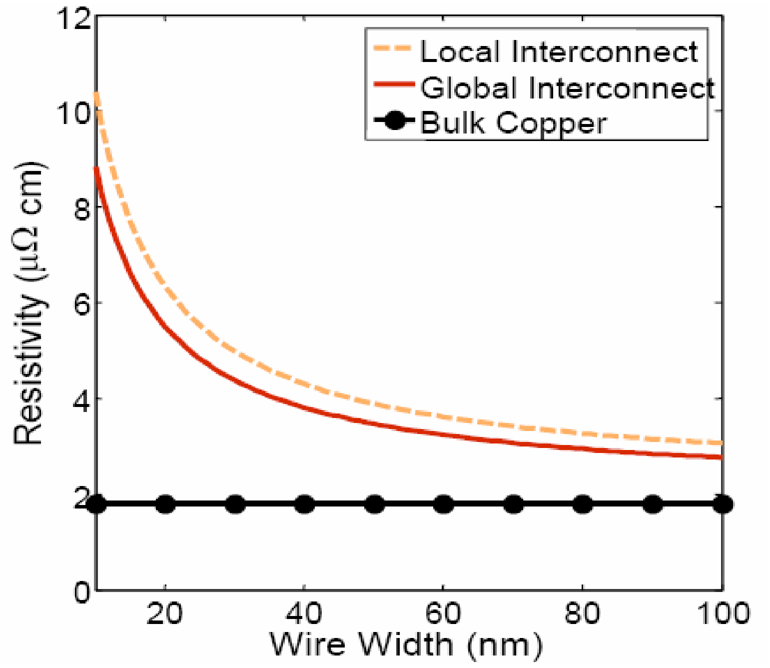
- Properties of carbon nanotubes (CNT)
- Predicting the performance of CNT interconnect
- Circuit model of CNT interconnect.
- Fault Model of CNT interconnect.
- Fabrication of Bundle CNT-interconnect.
- Conclusion.

# Interconnect and Technology scaling

- On chip communication is a bottleneck.
  - Copper interconnect currently plagued by delay, noise, and reliability problems
  - Electromigration also decreases reliability.
- Problem aggravated by interconnect scaling
  - Smaller wire dimensions
  - Process variations becoming an important reliability concern

# Resistivity changes in copper wire with Technology

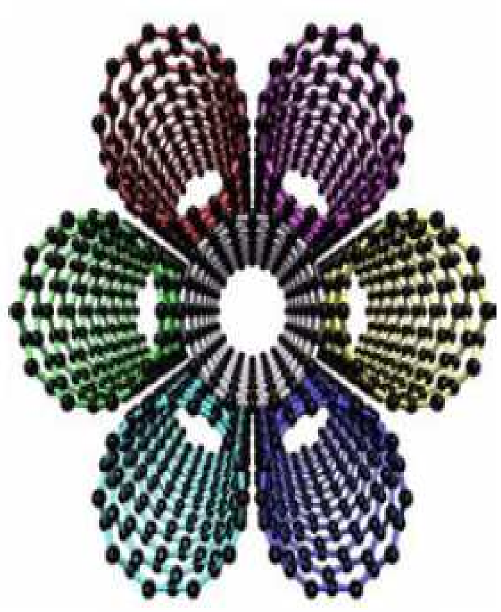
- Resistivity of copper interconnect increases as cross-sectional dimensions decreases( Dimensions on the order of mean free path of electrons).
- Radical alternative technology is required
- ITRS 2006.



# Carbon Nanotubes for On-chip Interconnects.

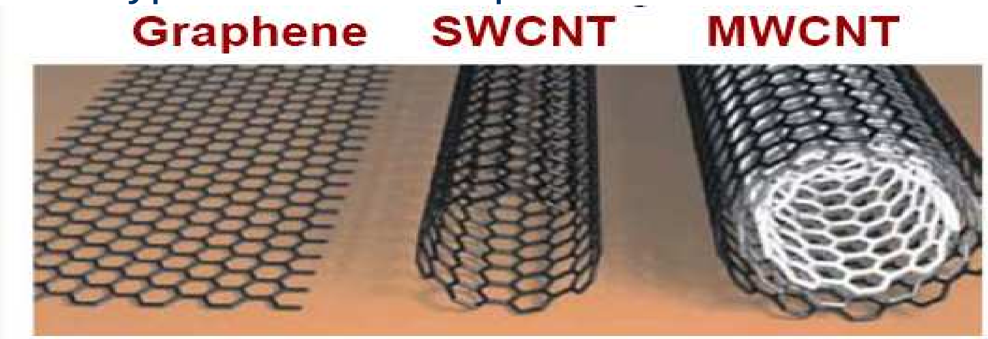
- Carbon nanotubes have been proposed as a possible replacement for on-chip interconnect.

1. Large current density.
2. Relatively low resistivity.
3. Small dimensionality



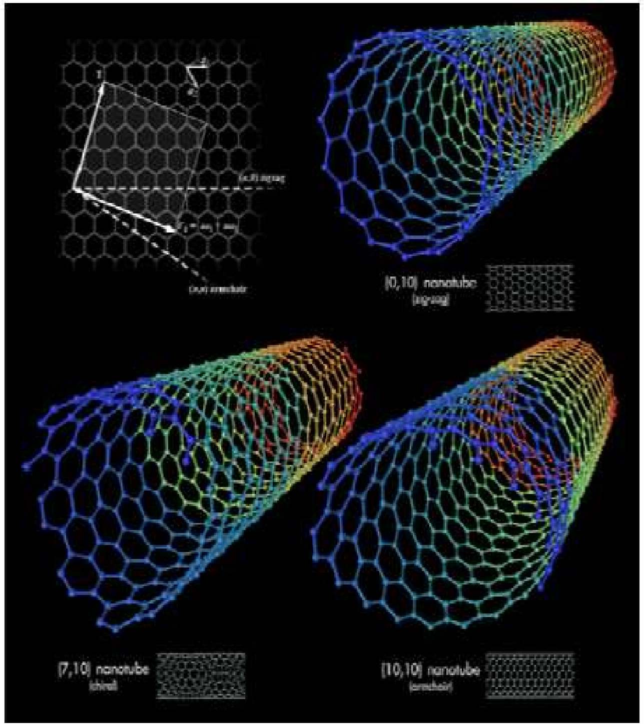
# Types of Carbon Nanotube

- Single-walled carbon nanotubes (SWCNTs).
1. Rolled single sheet of graphene.
2. Typical diameter: 0.4 nm to 4.0 nm.
- Multi-walled carbon nanotubes (MWCNTs).
1. Nested SWCNTs.
2. Distance between layers: 0.34 nm.
3. Typical diameter: up to 100 nm.



# Single Walled CNT: Electrical Properties.

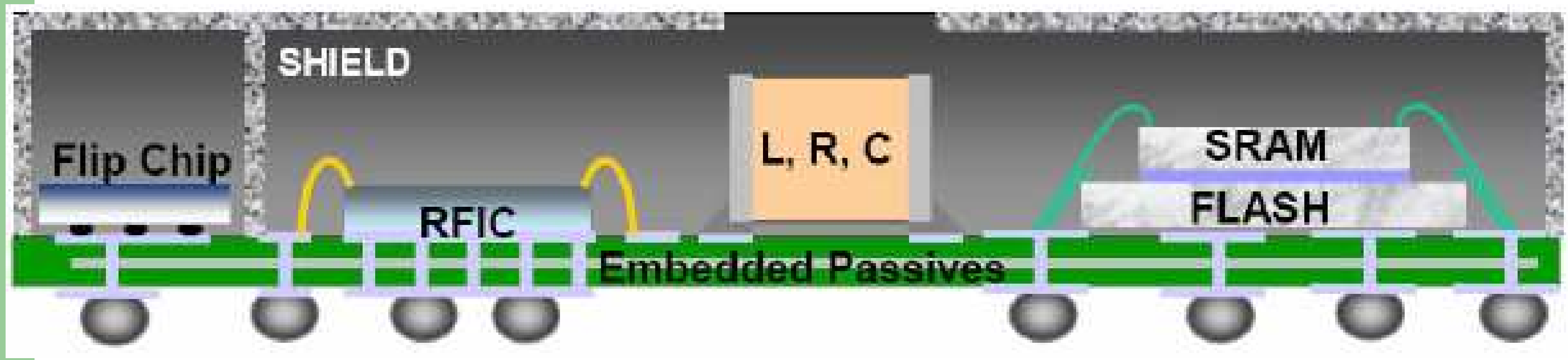
- SWCNTs exhibit either metallic or semiconducting behavior.
  - Chirality dependent.
  - 1/3 of possible SWCNT is Metallic.
- Strong carbon-carbon bonds allow large current densities ~ $10^9$ $A/cm^2$ .



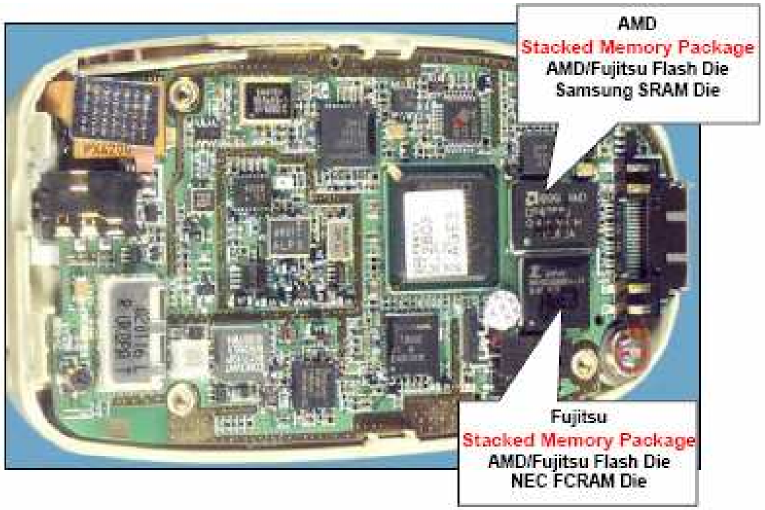
# Carbon nanotube Bundles

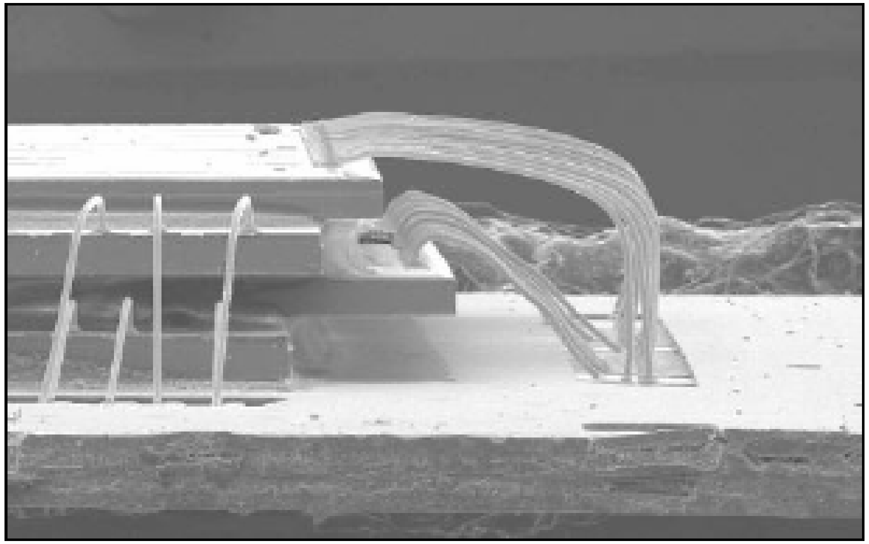
- Bundles of Carbon nanotubes have been proposed for interconnect applications.
- Why Bundles?
  - High Current carrying capabilites
  - Reduced resistance ( Single SWCNT has effective resistance of ~6.5K).
- Bundles of SWCNT have reduced resistance and effective inductance.

# System in Package



# SiP Integration Levels

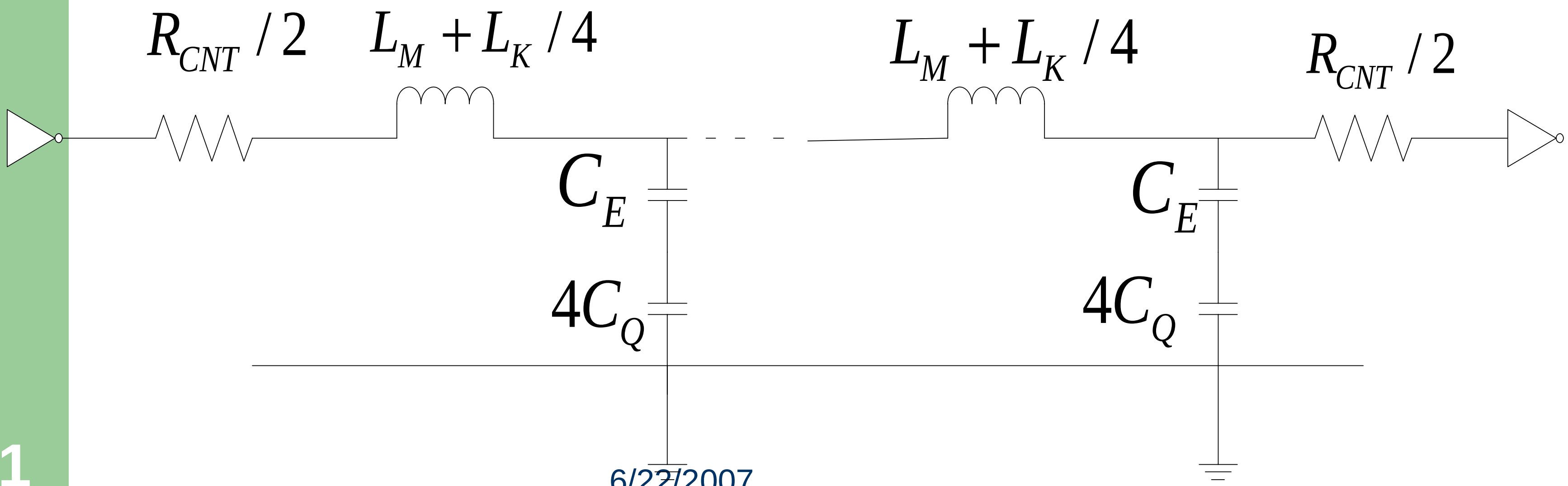


# Circuit model of SWCNT

- Equivalent circuit model for SWCNT bundles

1. Based on model for a single SWCNT from Burke [4].
2. Captures experimentally verified resistance as well as theoretically predicted capacitive and inductive effects.



# Electrostatic Capacitance

- To date, there is no accurate model to describe the electrostatic capacitive and inductive coupling between different CNT-bundles.
- The electrostatic capacitive and inductive couplings between CNT-bundles are strongly dependent on geometry, placement and distance of separation between individual CNT-bundle. They are also affected by permittivity and permeability of materials in different layers of SiP substrate in which these bundles are placed.
- Three Different models for determining Electrostatic capacitance between CNT-bundles.

# PROPOSED CNT BUNDLE MODEL

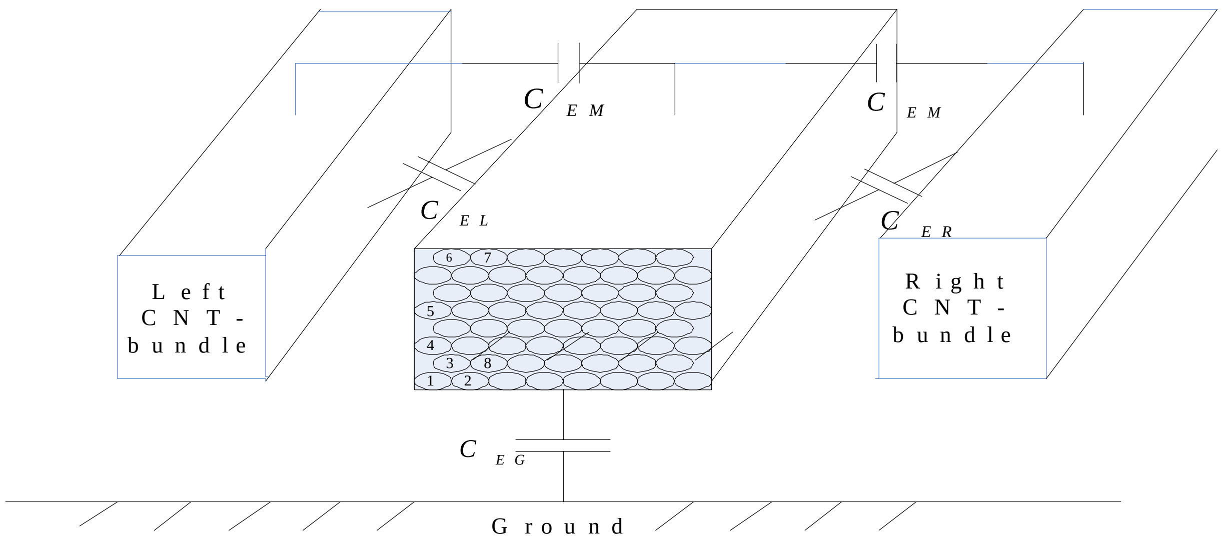
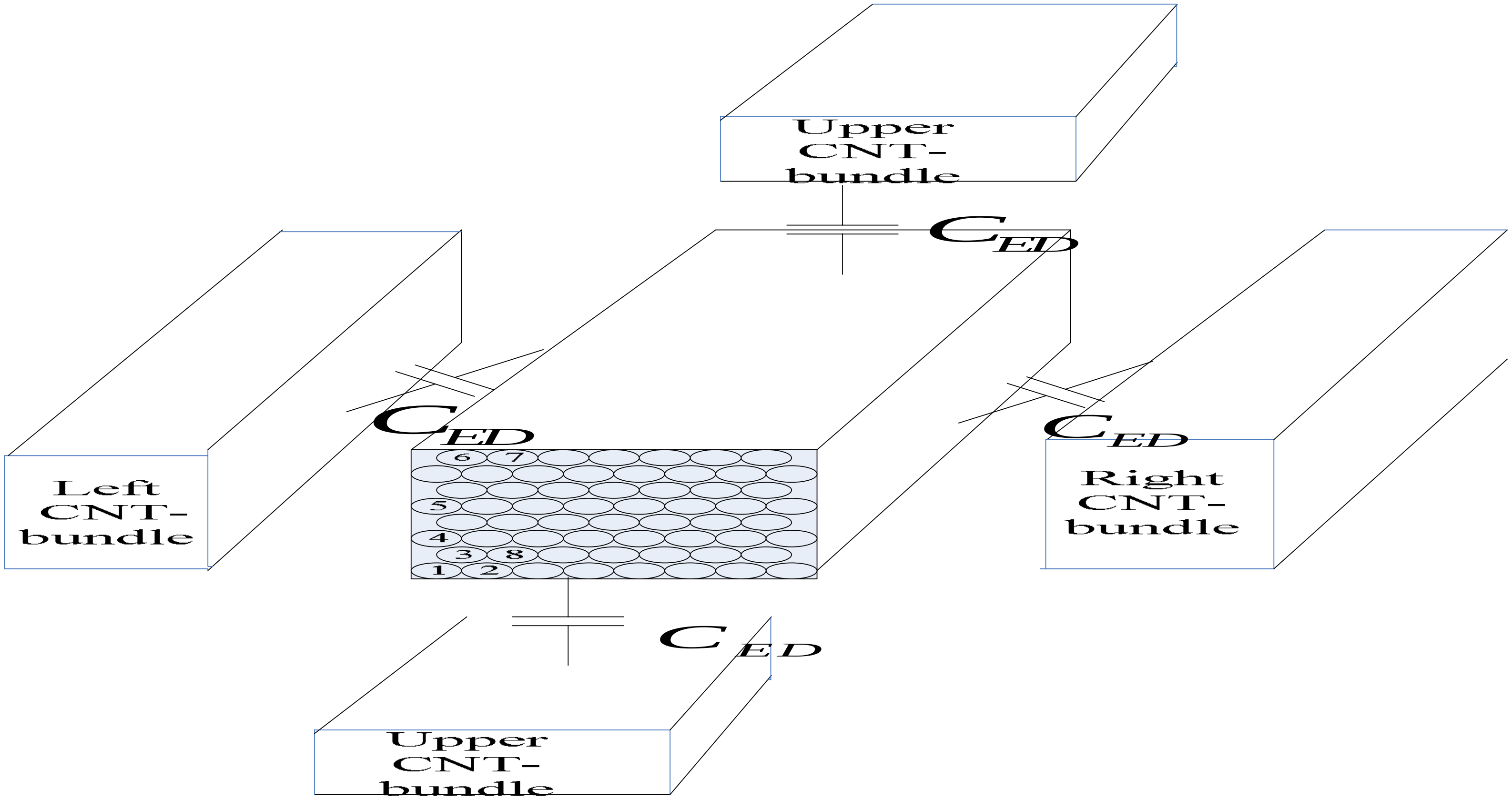
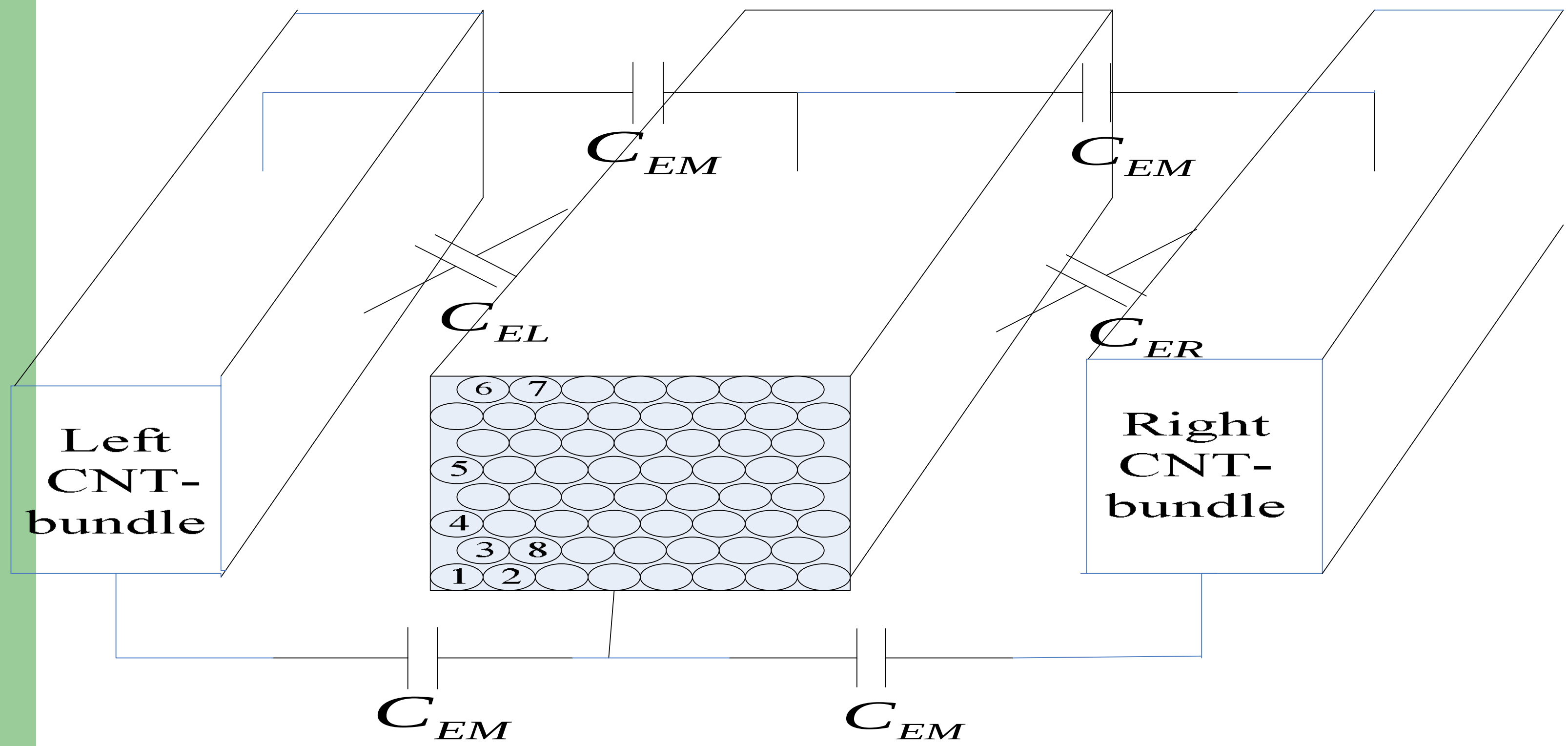



Fig. 1: Three CNT bundles in parallel with ground plane (geometry I).

# Stacked CNT Bundle Model



# Power Plane CNT-Bundle Model

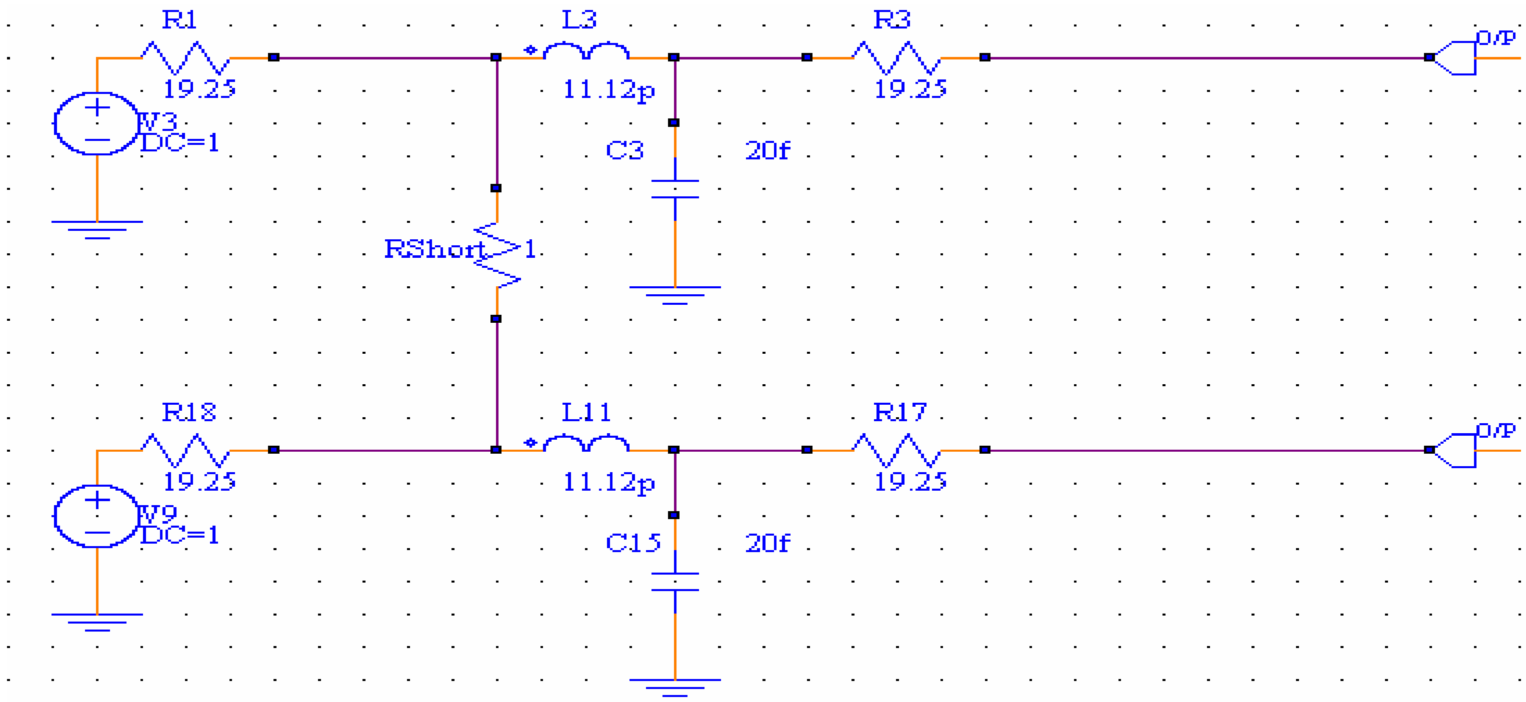


# Defects in CNT-bundle Interconnect

- CNT-bundle interconnects in nano scale SiP design is affected by various parametric variations, manufacturing defects and process variations .
- Types of Defects
  - Short Defects.
  - Open Defects.

# Shorts Defect Model

- A short defect is a connection between the two CNT-bundles that are merged and it forms a single bundle at a defective point.

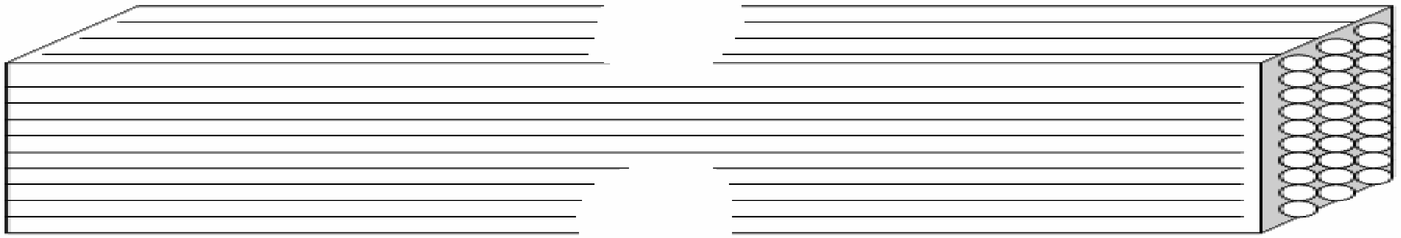


# OPEN DEFECTS

- An open defect is a break in the connection in the CNT-bundle. Two major types of open defects that are important from nano interconnects point of view are
  - Complete Open
  - Partial Open

# Physical Open Defects

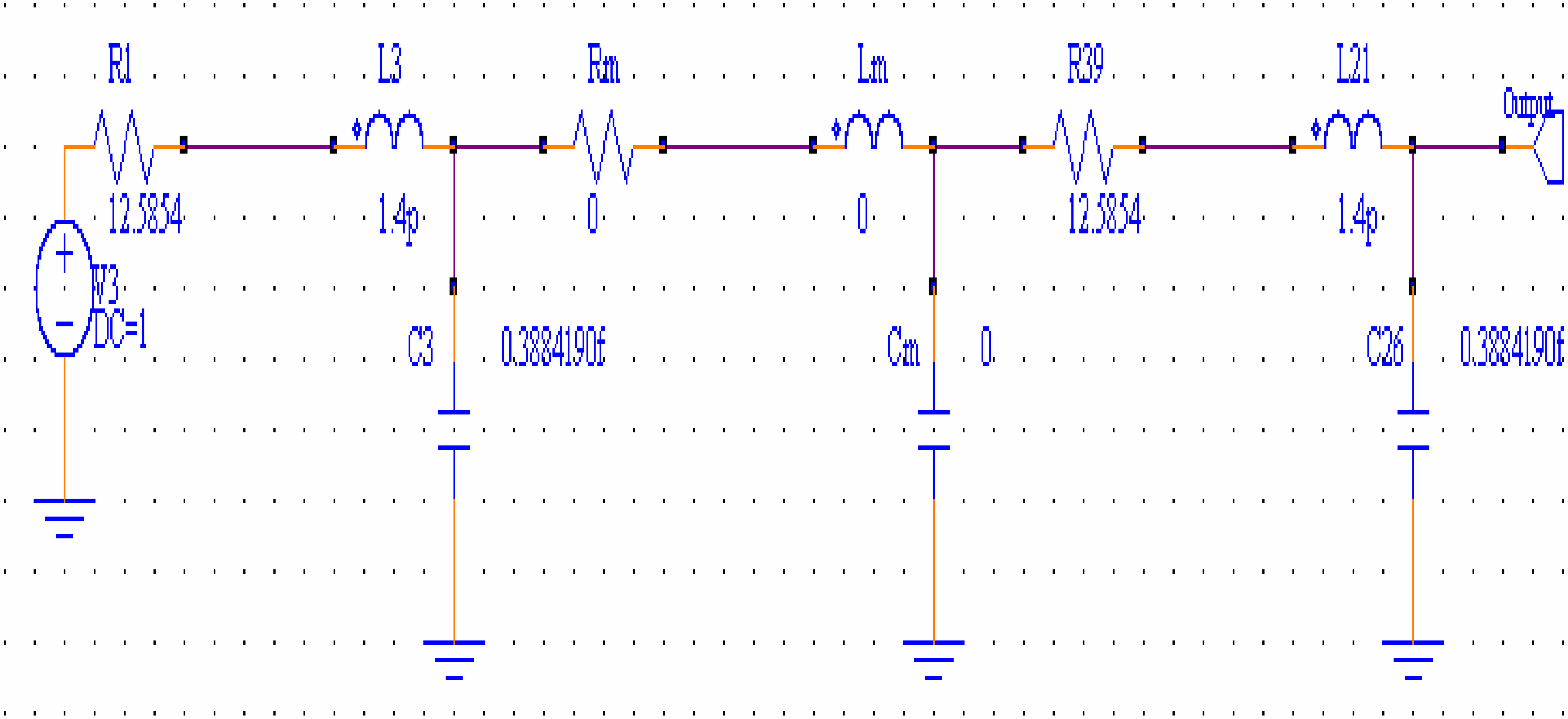
(a)



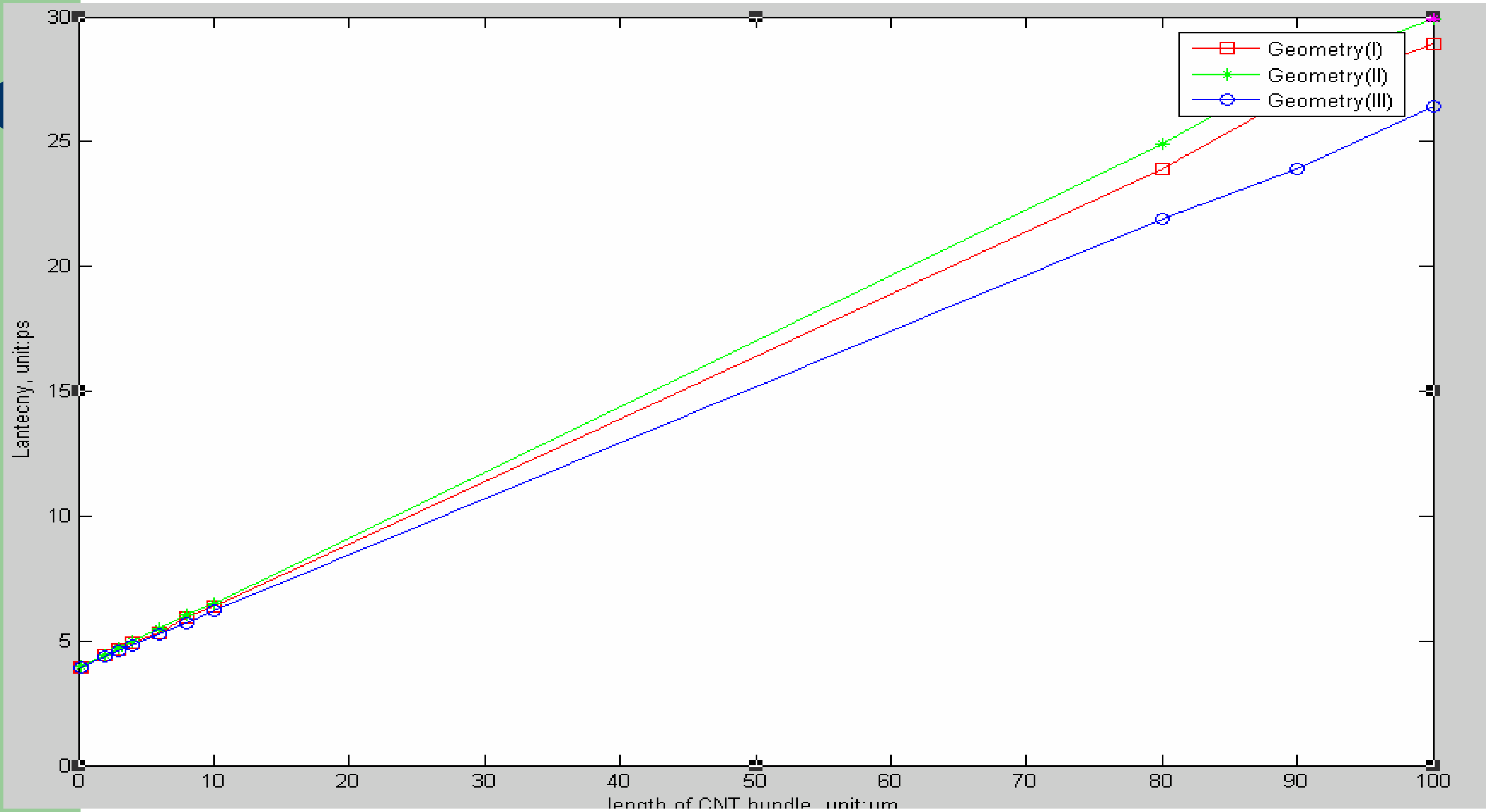
(b)

(c)

# OPEN DEFECT MODEL

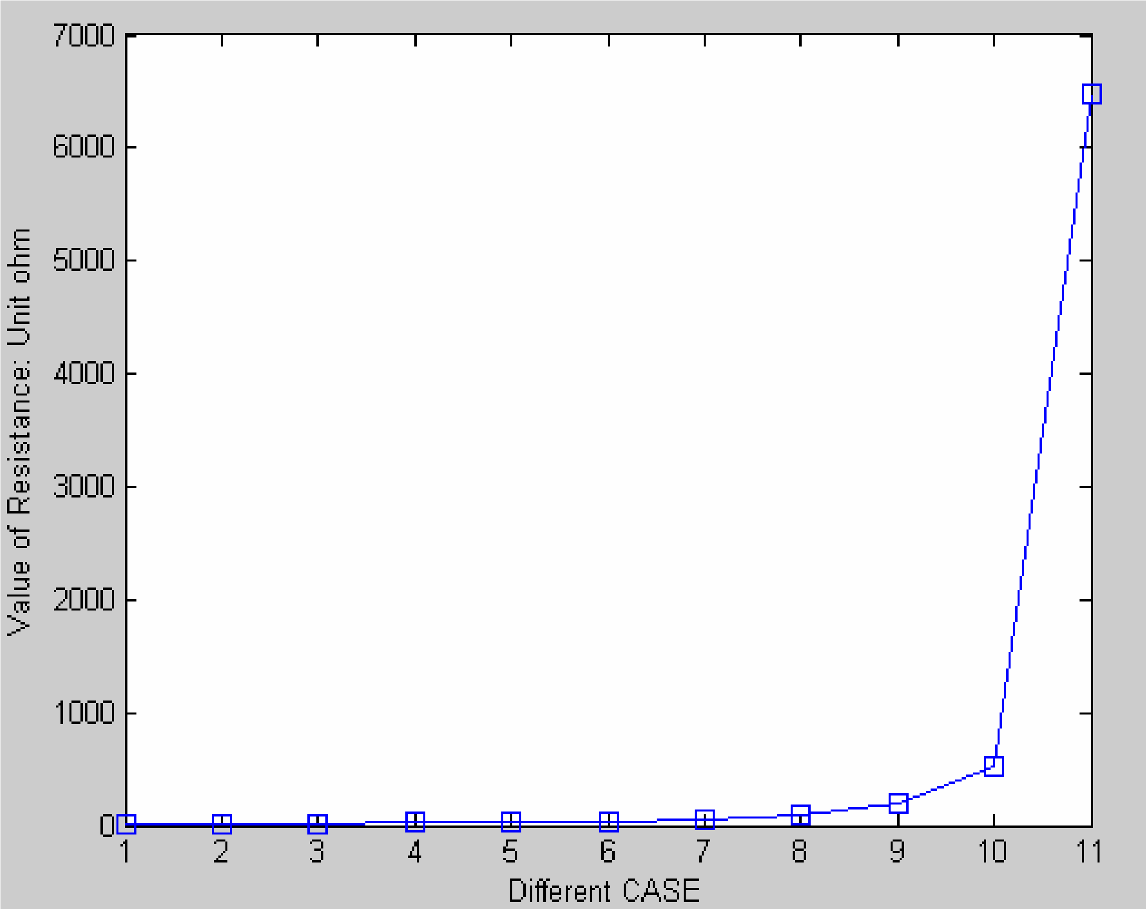


# Latency variation in CNT-bundles

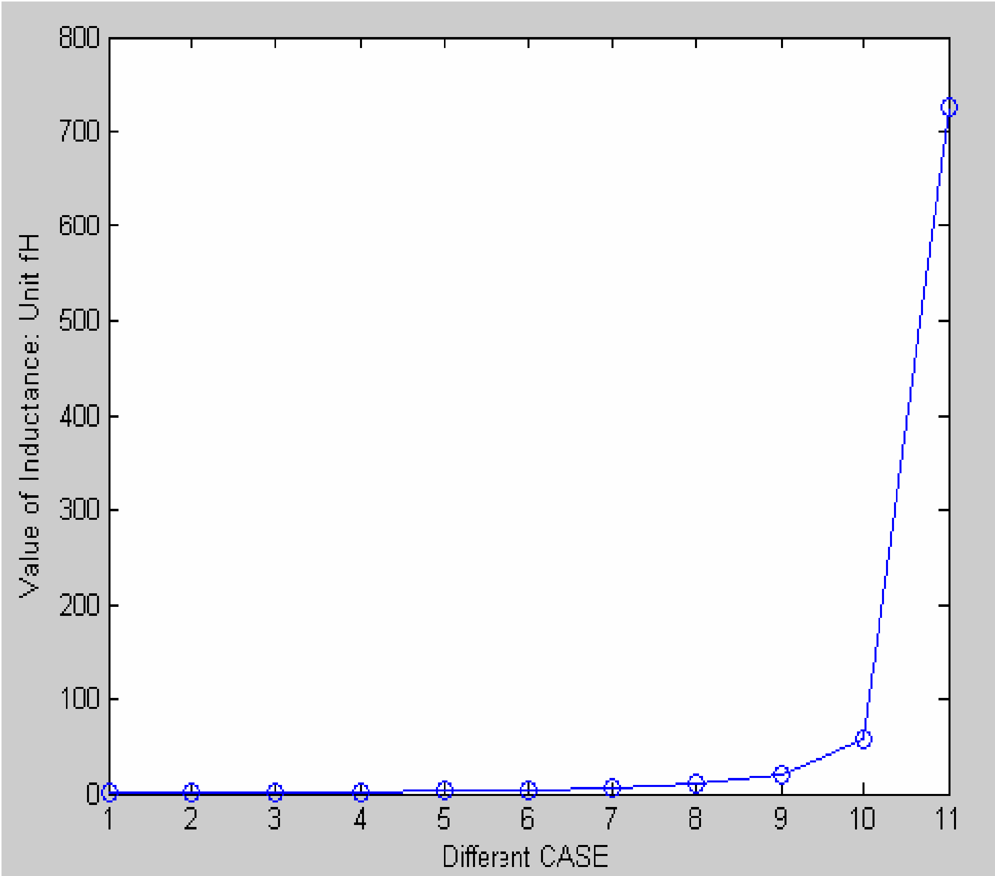



# CNT BUNDLE

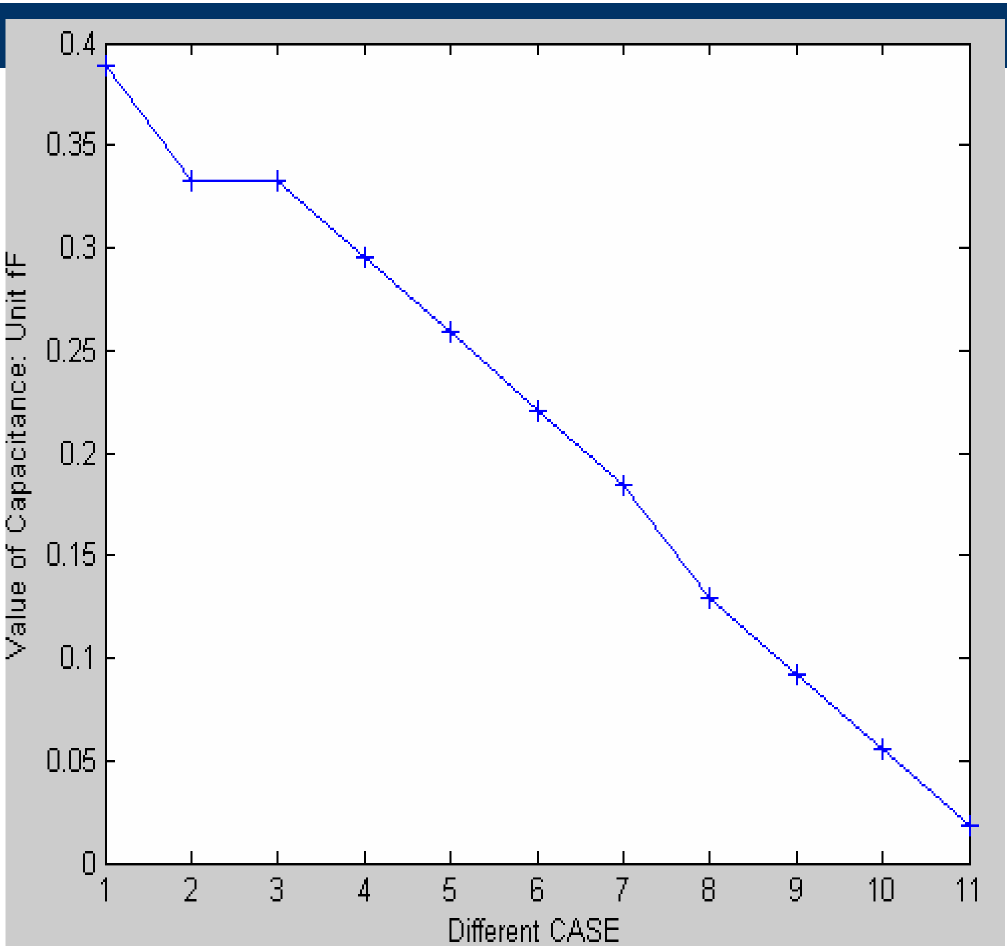
# variation of effective resistance



# Effective inductance



# Effective Capacitance



# CONCLUSIONS

- We proposed three different CNT-bundle architectures for nano scale interconnect applications in system-in-package.
- We compared the latency of the three architectures.
- We provided defect models of the CNT interconnects for open and shorts defects.
- Increase in resistance and inductance as the defect sizes increases whereas the effective capacitance decreases.

# REFERENCES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# Acknowledgement

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